LISTING OF THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application. Please amend the claims as follows:

1. (Previously Presented) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of groups of simulation processors having a plurality of outputs;

for each of the groups of simulation processors, a corresponding one of a plurality of first reconfigurable interconnect stages each having a plurality of inputs coupled to the outputs from only the corresponding group of simulation processors, and further having a plurality of outputs;

for each of the first reconfigurable interconnect stages, a corresponding one of a plurality of second reconfigurable interconnect stages each having a plurality of inputs coupled to a first subset of the outputs from only the corresponding first reconfigurable interconnect stage, and further having a plurality of outputs, wherein a first subset of the outputs from each second reconfigurable interconnect stage are coupled to a first subset of the inputs of only the corresponding first reconfigurable interconnect stage via a plurality of feedback paths;

a third reconfigurable interconnect stage having a plurality of inputs coupled to a second subset of the outputs from the second reconfigurable interconnect stages,

wherein the plurality of feedback paths each couples one of the outputs of the second reconfigurable interconnect stages to one of the inputs of the first reconfigurable interconnect stages without passing through the third reconfigurable interconnect stage; and

memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the first, second, and third reconfigurable interconnect stages in accordance with a content of the memory.

2. (Previously Presented) The reconfigurable interconnect network of claim 1, wherein a second subset of the outputs from each of the first reconfigurable interconnect stages are coupled to inputs of the corresponding group of simulation processors.

3. (Canceled)

4. (Previously Presented) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of clusters, each cluster including:

a plurality of simulation processors, and

a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors in the cluster;

a second reconfigurable interconnect stage configurable to receive a first plurality of outputs from the first reconfigurable interconnect stages and to provide a first plurality of outputs back to inputs of the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive a second plurality of outputs of the second reconfigurable interconnect stage and to provide outputs back to inputs of the clusters,

wherein the first plurality of outputs of the second reconfigurable interconnect stage is each coupled to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage; and

memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the first, second, and third reconfigurable interconnect stages in accordance with a content of the memory.

5. (Previously Presented) The reconfigurable interconnect network of claim 4, wherein the first reconfigurable interconnect stage is further configurable to provide a second plurality of outputs back to inputs of the simulation engines of the clusters.

6. (Previously Presented) In a logic simulation system, a reconfigurable interconnect network comprising:

a first reconfigurable interconnect stage;

a second reconfigurable interconnect stage configurable to receive outputs from the first reconfigurable interconnect stage and to provide a first plurality of outputs back to inputs of the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive a second plurality of outputs from the second reconfigurable interconnect stage and provide outputs back to the first reconfigurable interconnect stage,

wherein the first plurality of outputs of the second reconfigurable interconnect stage is each coupled to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage; and

memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the first, second, and third reconfigurable interconnect stages in accordance with a content of the memory.

7. (Original) The reconfigurable interconnect network of claim 6, wherein the first reconfigurable interconnect stage is coupled to outputs from a plurality of simulation processors.

8. (Previously Presented) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of groups of simulation processors;

for each of the groups of simulation processors, a corresponding first reconfigurable interconnect stage having a first plurality of inputs coupled to outputs of only the corresponding group of simulation processors;

for each of the first reconfigurable interconnect stages, a corresponding second reconfigurable interconnect stage having a first plurality of inputs coupled to outputs of only the corresponding first reconfigurable interconnect stage and a first plurality of outputs coupled to a second plurality of inputs of only the corresponding first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage having inputs coupled to a second plurality

of outputs of the second reconfigurable interconnect stages, and further having outputs coupled to a second plurality of inputs of the second reconfigurable interconnect stages,

wherein the first plurality of outputs of each of the second reconfigurable interconnect stages is each coupled to one of a second plurality of inputs of the corresponding first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage; and

memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the first, second, and third reconfigurable interconnect stages in accordance with a content of the memory.

9. (Previously Presented) The reconfigurable interconnect network of claim 8, wherein the second plurality of outputs of the second reconfigurable interconnect stages are coupled to the inputs of the third reconfigurable interconnect stage using a butterfly topology.

10. (Previously Presented) The reconfigurable interconnect network of claim 8, wherein each of the second and third reconfigurable interconnect stages comprises a crossbar.

Claims 11-24. (Canceled).